CLAIMS

I CLAIM:

1. A circuit comprising:

a first circuit having a first input and a first output, said first output being a function of said first input plus a noise component;

a second circuit, identical to and located proximate to said first circuit, and having a second input and a second output;

said second input set to cause said second output to equal said noise component of said first output; and

a subtractor circuit connected to said first circuit and to said second circuit to subtract said second output from said first output.

2. A circuit according to claim 1 further comprising a digital circuit located proximate to said first circuit and to said second circuit.

3. A circuit according to claim 1 wherein said subtractor circuit further comprises a halving circuit.

4. A circuit comprising:

a first circuit having a first input and a first output, said first output being a function of said first input plus noise;

a second circuit, identical to said first circuit, and having a second input and a second output;

said second input ~~designed~~ set to cause said second circuit to produce, as said second output, said noise only; and

a third circuit having a third input connected to said first output, a fourth input connected to said second output to subtract said second output from said first output.

5. A circuit according to claim 4, further comprising a digital circuit proximal to said first circuit and to said second circuit.

6. A circuit according to claim 5, wherein said first circuit, said second circuit, said third circuit, and said digital circuit are on a single integrated circuit chip.

7. A circuit comprising:

a first circuit having a first input and a first output, said first output being a function of said first input plus noise;

a second circuit, identical to said first circuit, and having a second input and a second output;

said second input, being an inverse of said first input, ~~causing~~ causal said second circuit to produce, as said second output, an inverse function of said first circuit plus noise; and

a third circuit having a third input connected to said first output and a fourth input connected to said second output, and combining said second output from said first output.

8. A circuit according to claim 7 wherein said third circuit further comprises a halving circuit.

9. A circuit according to claim 7, further comprising a digital circuit proximal to said first circuit and to said second circuit.

10. A circuit according to claim 9, wherein said first circuit, said second circuit, said operator circuit, and said digital circuit are on a single integrated circuit chip.

11. An integrated circuit chip (IC) circuit comprising:

a digital circuit;

a plurality of analog circuits, each proximal to said digital circuit and to each other, and each of said plurality of analog circuits producing an output signal;

a noise detector circuit, proximal to said plurality of analog circuits, and producing a noise signal;

a noise canceling circuit, processing said outputs from said plurality of analog circuits with said noise signal.

12. An IC according to claim 11 wherein said noise canceling circuit comprises a subtractor circuit.

13. An IC according to claim 11 wherein said noise canceling circuit further comprises a halving circuit.

14. A noise cancellation method comprising the steps:

supplying a first signal to a first circuit;

reading a first output from said first circuit;

supplying a null signal to a second circuit located proximal to said first circuit;

reading a second output from said second circuit;

combining said first output with said second output to produce a combinational output.

15. A method according to claim 14 wherein said second circuit is identical to said first circuit.

16. A method according to claim 14 wherein said step of combination comprises the step of subtracting said second output from said first output.

17. A method according to claim 14 wherein said step of combination comprises the step of adding said second output to said first output.

18. A method according to claim 17 wherein said step of combination further comprises the step of halving said added output.

19. A method to minimize effects of digital circuit noise on analog circuits, said method comprising the steps:

supplying a first signal to a first analog circuit;

reading a first output from said first analog circuit;

supplying a second signal to a second analog circuit;

reading a second output from said second analog circuit;

supplying a null signal to a third analog circuit located proximal to said first analog circuit and to said second analog circuit;

reading a third output from said third analog circuit;

combining said first output with said third output to produce a first combinational output; and combining said second output with said third output to produce a second combinational output.